AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph at page 1, lines 4-9, as follows:

This application is related to Application No. ~~(L13.12 0172/00 629)~~10/017,792 filed ~~on even date herewith~~December 12, 2001 for "Optimization of Comparator Architecture" by Sergej B. Gashkov, Alexander E. Andreev and Aiguo Lu and assigned to the same assignee as the present invention, which application is incorporated herein by reference.

Please amend the paragraph at page 3, lines 4-19, as follows:

In one embodiment, an adder based circuit is embodied in an integrated circuit. The adder based circuit comprises an input module that receives inputs A[i] and B[i] to generate U[i] = A[i]&B[i] and either V[i] = A[i]$\lor$B[i] or V[i] = A[i]$\oplus$B[i]. A carry module is responsive to U[i] and V[i] to generate carry functions. An output module is responsive to the U[i], V[i] and carry functions to provide an output function $S = \sum_{i=0}^{n-1} 2^i S[i]$ $S = \sum_{i=0}^{n} 2^i S[i]$

$= \sum_{i=0}^{n-1} 2^i A[i] + \sum_{i=0}^{n-1} 2^i B[i]$. The carry module has a minimal depth defined by a recursive expansion of at least one carry function associated with the carry module based at least in part on a variable k, where k = F_l and n-k = F_{l-1} and where l satisfies F_l < n $\leq$ F_{l+1}, {F_l} is a Fibonacci series and n is the number of bits of at least one of U[i] and V[i].

Please amend the paragraph at page 4, lines 3-17 as follows:

In one embodiment, recursive functions are defined as h'_l =

h_1(U[k+1],U[k+2],V[k+2],...,   U[k+1],V[k+1])   and   v'_1   = V[k+1]&,...,&V[k+1], based on the carry functions, where k=F_1 and n-k=F_{1-1}, 1 satisfies $F_1 < n \leq F_{\{1+1\}}$, {F_1} is the Fibonacci series defined recursively from the equality F_{1+1}=F{1}+F_{1+1} and n is the number of bits of an input to the carry module.   The recursive functions are recursively expanded to minimize 1.

Please amend the paragraph at page 4, line 27 to page 5, line 9 as follows:

In other embodiments, the fanout depth of the adder based circuit is minimized by defining recursive functions

$$H^i_k = h^{\{i+1\}}_{\{k-1\}} \vee v^{\{i+1\}}_{\{k-1\}} \& h^i_1$$

and

$$v^i_1 = v^{\{i+1\}}_{\{k^1\}} \& v^i_1$$

based on the output function,

where k=F_1 and n-k=F_{1-1}, 1 satisfies $F_1 < n \leq F_{\{1+1\}}$, {F_1} is the Fibonacci series defined from the equality F_{1+1}=F{1}+F_{1+1}.   The recursive functions are recursively expanded to minimize 1.

Please amend the paragraph at page 17, line 27 to page 18, line 16 as follows:

As in the convention adopted in the aforementioned Gashkov et al, application, if k is selected as the left extremity of a series (least allowable value), the a circuit is referred to as a left-side circuit; if k is selected as the right extremity of this series (greatest allowable value), the circuit is called right-side circuit.   Also as described in the Gashkov et al. application, it is possible to distribute negations and execute other technological mapping techniques to derive 2-input elements

in place of 3-input elements forming circuits that are topologically the same based on the following identities

$$h_{k+1} = \neg(\neg h'_1) \lor v'_1 \& h_k$$
$$= NAND(\neg h'_1, ND(v'_1, h_k)),$$
$$\neg h_{k+1} = \neg(h'_1 \lor v'_1, h_k)$$
$$= AO6(v'_1, h_k, h'_1), \text{ and}$$
$$V_{k+1} = v_{1,k} \& v_k, \text{ where } AO6(a,b,c) = NOR(AND(a,b),c).$$

Please amend the paragraph at page 20, lines 17-24 as follows:

Minimization of the depth of circuit HV_n is carried out, by considering $U[i] = 1$, for $0 \leq i \leq n-i$ with the help of the optimal choice of parameter k in each step of recursive construction of HV_n from modules HV_{k}, HV_{n-k} and their connecting modules. The connecting modules consist of the parallel modules GP which are assumed, for example, to be formed from 2-input elements.